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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,345	12/29/2003	Mark L. Doczy	42P17820	8139

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN  
12400 WILSHIRE BOULEVARD  
SEVENTH FLOOR  
LOS ANGELES, CA 90025-1030

EXAMINER

THAI, LUAN C

ART UNIT PAPER NUMBER

2891

DATE MAILED: 06/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/748,345

Applicant(s)

DOCZY ET AL.

Examiner

Luan Thai

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 04 May 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election *without traverse* of Group II, claims 1-16, filed 5/4/05 is acknowledged.

Claims 17-24 are canceled.

### *Claim Objections*

2. Claims 2-4, 5, 8-10, and 13-16 are objected to because of being redundant. For example:

In claim 2, the phrase "*wherein providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer disposed on a gate dielectric layer comprising providing a substrate comprising source/drain and gate regions, wherein the gate region comprises a metal layer comprising ...*" is considered to be redundant and not clear. Similar redundant phrase also appear in claims 3-4, 8-10, and 13-16.

In claim 5, the comma "." after the word "substrate" should be deleted.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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4. Claims 1-5 and 7-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsukamoto (6,040,224).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 3-5, 7, 9-10, and 14, Tsukamoto (see specifically figure 5C-5E) disclose a method of forming a microelectronic structure comprising: providing a substrate (11) comprising source/drain regions (21) and gate region (18), wherein the gate region comprises a metal layer (15) of tungsten disposed on a gate oxide layer (13) considered as a high-k dielectric layer, a polysilicon layer (16) disposed on the metal layer (15), and laser annealing the substrate to activate the implanted species (Col. 4, lines 65+), wherein the metal layer does not substantially diffuse into the gate dielectric layer or to the polysilicon layer disposed on the metal layer (Col. 6, lines 1-16).

Regarding claims 2, 11, and 13, since the metal layer (15) made of tungsten, it inherently comprises a work function about 4eV, as evidenced by Bustos et al. (U.S. 2004/0126977, paragraph [0067]); and thus, the work function of layer (15) is approximately equal to the work function of a doped polysilicon, as evidenced by Applicant's Specification, paragraph [0018].

Regarding claims 8 and 12, Tsukamoto's figures 5D-5E show the ratio of the depth of the source/drain regions (21) to the length of the source/drain regions (21) being less than about 1:2.

5. Claims 1-3, 5, 7-9, and 11-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang (US 2002/0105033).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 3, 5, 7, 9, and 14, Zhang (see specifically figure 1A) disclose a method of forming a microelectronic structure comprising: providing a substrate (1) comprising source/drain regions (24) and gate region (6/8), wherein the gate region comprises a metal layer (8) disposed on a gate high-k dielectric layer (6) (paragraph [0063]), and laser annealing the substrate to activate the implanted species (paragraph [0071]), wherein the metal layer does not substantially diffuse into the gate dielectric layer (paragraphs [0064]-[0065] and [0072]-[0073]).

Regarding claims 2, 11, and 13, since the gate electrode (8) may be made of Si, which comprises a work function about 4eV, as evidenced by Das et al. (U.S. Patent No. 5,627,427, Col. 2, lines 4+), the work function of the Si layer (8) is approximately equal to the work function of a doped polysilicon, as evidenced by Applicant's Specification, paragraph [0018].

Regarding claims 8 and 12, Zhang's figure 1A shows the ratio of the depth of the source/drain regions (24) to the length of the source/drain regions (24) being less than about 1:2.

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto (6,040,224) in view of Bustos et al. (U.S. 2004/0126977).

Regarding claim 15, Zhang discloses the claimed invention as detailed above except for specifying the work function range of the metal layer (e.g., from about 4.8 to about 5.1 electron volts).

Bustos et al. teach that for P-type MOS transistor, a metal having a work function of about 5.3 electron volts is particularly suitable, such as platinum, palladium, ruthenium, etc. (paragraph [0067]). It would have been obvious to one of ordinary skill in the art at the time the invention was made to select the materials, as taught by Bustos et al., since such material having a suitable work function for forming a P-type MOS transistor. And although the proposed method of Tsukamoto and Bustos et al. does not explicitly teach exact the work function range as claimed, such range is an art recognized variable of importance which is subject to routine experimentation and optimization.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto (6,040,224) in view of Halliyal et al. (6,783,591).

Regarding claim 16, Zhang discloses the claimed invention as detailed above except for specifying the gate oxide layer being selected from the group consisting of hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide.

It should be noted that the materials such as hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide are widely used for forming the gate oxide layer in a gate electrode structure, as disclosed by Halliyal et al. (Col. 8, lines 35+), since such materials have a suitable high-k dielectric for the process forming the structure (Col. 4, lines 14-23).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to select the materials, taught by Halliyal et al., in forming the gate oxide layer in Tsukamoto's gate structure, in order to have a suitable high-k dielectric for the process.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto (6,040,224) in view of Goto (6,599,819).

Regarding claim 6, Tsukamoto discloses the claimed invention as detailed above except for specifying the laser beam pulsed at about 20 nanoseconds or less.

Although Tsukamoto does not specify the time range of the laser beam pulsed (e.g., 20 nanoseconds or less), the annealing time using laser beam is commonly less than 20 ns for activating the implanted regions in a substrate, as disclosed by Goto (Col. 3, lines 49+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to pulse the laser beam to the substrate at about 20 ns or less for activating the implanted regions in the substrate since such the pulsed time of a laser beam is commonly applied in the art, as taught by Goto, and such time range is an art recognized variable of importance which is subject to routine of experimentation and optimization.

10. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 2002/0105033).

Regarding claim 15, Zhang discloses the claimed invention as detailed above except for specifying the work function range of the metal layer (e.g., from about 4.8 to about 5.1).

Although Zhang does not specify the work function range of the metal layer as applicant claimed, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the metal layer having the work function in the claimed range because the work function range is an art recognized variable of importance which is subject to routine of experimentation and optimization.

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11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 2002/0105033) in view of Goto (6,599,819).

Regarding claim 6, Zhang discloses the claimed invention as detailed above except for specifying the laser beam pulsed at about 20 nanoseconds or less.

Although Zhang does not specify the time range of the laser beam pulsed (e.g., 20 nanoseconds or less), the annealing time using laser beam is commonly less than 20 ns for activating the implanted regions in a substrate, as disclosed by Goto (Col. 3, lines 49+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to pulse the laser beam to the substrate at about 20 ns or less for activating the implanted regions in the substrate since such the pulsed time of a laser beam is commonly applied in the art, as taught by Goto, and such time range is an art recognized variable of importance which is subject to routine of experimentation and optimization.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available



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A handwritten signature in black ink, appearing to read 'Luan Thai', with a long horizontal flourish extending to the right.

**Luan Thai**

**Primary Examiner**

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May 13, 2005